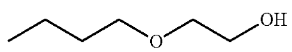
[Chemical Formula 1]



[0051] The coating layer **400** may reduce or prevent a short circuit from being formed between the outer terminals **150** and between the outer terminals **150** and the shielding layer **500**.

[0052] The shielding layer may be provided on the mold layer **300**. The shielding layer **500** may be provided to cover top and side surfaces **300***a* and **300***b* of the mold layer **300** and the side surfaces **100***c* of the substrate **100**. The shielding layer **500** may be connected to the ground pattern **105** exposed through the side surfaces **100***c* of the substrate **100**. The shielding layer **500** may be formed of or include at least one of, for example, copper (Cu), nickel (Ni), silver (Ag), gold (Au), platinum (Pt), cobalt (Co), titanium (Ti), chromium (Cr), zirconium (Zr), molybdenum (Mo), tungsten (W), ruthenium (Ru), hafnium (Hf), or rhenium (Re).

[0053] The shielding layer **500** may reduce or prevent an electromagnetic wave from propagating into or from an electronic device (e.g., mobile devices, computers, and so forth). The shielding layer **500** may be electrically connected to the ground pattern **105** of the substrate **100**, and this connection may allow an electromagnetic wave incident thereon to be transmitted to the outside. Furthermore, since the shielding layer **500** may be formed of or include a conductive material, it is possible to better dissipate heat energy generated in the semiconductor package **1** to the outside.

[0054] FIGS. **2**A to **2**E are sectional views illustrating a method of fabricating a semiconductor package, according to example embodiments of the inventive concepts.

[0055] Referring to FIG. **2**A, semiconductor chips **200** may be mounted on a substrate **100**, and a mold layer **300** may be formed to cover the semiconductor chips **200**. The substrate **100** may be a strip type structure, on which a plurality of semiconductor chips **200** are provided. The substrate **100** may be a printed circuit board (PCB) that has a top surface **100***a* and a bottom surface **100***b* facing each other and includes circuit patterns. The semiconductor chips **200** may be spaced apart fro each other on the top surface **100***a*, and may be connected to the substrate **100** by a wire bonding method. The adhesive layers **220** may be provided between the top surface **100***a* of the substrate **100** and the semiconductor chips **200**. The mold layer **300** may be formed to cover the top surface **100***a* of the substrate **100** and the semiconductor chips **200**. For example, the mold layer **300** may be formed by a mold under-fill (MUF) process. The mold layer **300** may be formed of or include an insulating polymer material (e.g., epoxy molding compound (EMC)).

[0056] Referring to FIG. **2**B, outer terminals **150** may be attached to connection pads **120**. The outer terminals **150** may be formed of or include an alloy including at least one of tin (Sn), silver (Ag), copper (Cu), nickel (Ni), bismuth (Bi), indium (In), antimony (Sb), and cerium (Ce). The connection pads **120** may be electrically connected to the outer terminals **150**.

[0057] Referring to FIG. **2**C, a coating layer **400** may be formed to cover the bottom surface **100***b* of the substrate **100**, the connection pads **120**, and the outer terminals **150**. The coating layer **400** may be formed to substantially entirely cover the exposed surfaces of the outer terminals **150**. The coating layer **400** may be formed by a method of spraying a water-soluble material or by a method of dipping the bottom surface **100***b* of the substrate **100** and the outer terminals **150** into solution containing a water-soluble material. The water-soluble material may be dissolved in water at a temperature of about 50° C. or higher. For example, the water-soluble material may contain 2-Butoxyethanol.

[0058] Referring to FIG. **2**D, a cutting process may be performed on the substrate **100** and the mold layer **300** to separate the semiconductor chips **200** from each other. The cutting process may be performed using a saw blade or laser cutting technique. When the cutting process is finished, the mold layer **300** may have a top surface **300***a* and side surfaces **300***b*, and the substrate **100** may have side surfaces **100***c* exposing a ground pattern **105**.

[0059] Referring to FIG. **2**E, the shielding layer **500** may be formed to cover the mold layer **300** and the side surfaces **100***c* of the substrate **100**. The shielding layer **500** may be formed to cover top and side surfaces **300***a* and **300***b* of the mold layer **300** and the side surfaces **100***c* of the substrate **100**. The shielding layer **500** may be formed by a sputtering process, an electroplating process, or an electroless plating process. The shielding layer **500** may be formed of or include at least one conductive material such as, copper (Cu), nickel (Ni), silver (Ag), gold (Au), platinum (Pt), cobalt (Co), titanium (Ti), chromium (Cr), zirconium (Zr), molybdenum (Mo), tungsten (W), ruthenium (Ru), hafnium (Hf), or rhenium (Re). As a result, the semiconductor package **1** with the shielding layer **500** may be fabricated.

[0060] During the formation of the shielding layer **500**, a conductive material of the shielding layer **500** may be infiltrated into the outer terminals **150** provided on the bottom surface **100***b* of the substrate **100**, thereby causing occurrence of a short circuit therebetween. According to example embodiments of the inventive concepts, the coating layer **400** may be formed to cover the bottom surface **100***b* of the substrate **100** and the outer terminals **150**, thereby substantially preventing the conductive material from being infiltrated into the bottom surface **100***b* of the substrate **100** and the outer terminals **150**. Accordingly, when the coating layer **400** is formed, it is possible to substantially prevent a short circuit from being formed between the shielding layer **500** and the outer terminals **150**, without any additional process for protecting the outer terminals **150**. In addition, since the coating layer **400** is formed of or include a water-soluble material, the coating layer **400** can be easily removed.

[0061] FIGS. **3**A and **3**B are sectional views illustrating a method of connecting a semiconductor package to a board, according to example embodiments of the inventive concepts. FIGS. **3**A and **3**B are sectional views illustrating subsequent steps, which may be performed after the process steps described with reference to FIGS. **2**A to **2**E.

[0062] Referring to FIG. **3**A, a cleaning process may be performed on the coating layer **400**, which is formed on the bottom surface **100***b* of the substrate **100** and the outer terminals **150**. The cleaning process of the coating layer **400** may include a water jet process and a water dipping process. For example, water at a temperature of about 50° C. or higher may be supplied on the coating layer **400**, and in this case, the coating layer **400** may be removed via a hydrolysis reaction with the water.